

DR. MADHUSUDHANA K



PROFILE SUMMARY

Associate Professor and HOD with over 19 years of experience in teaching, research and industry

CONTACT DETAILS

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RESEARCH PROFILE

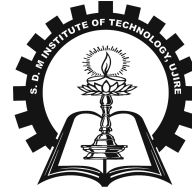
ORCID: 0000-0003-3666-3503
RESEARCHER ID: 102215069
Google Scholar ID: qbSzJKAAAAAJ
Linkedin ID:
dr-madhusudhana-k-87928682
IEEE Senior Member
MISTE

RESEARCH METRICS

• Citations:	20
• h-index:	3
• i10-index:	1

SKILLS

- Verilog, VHDL, Python, C, C++, NCTUNS, Xilinx, CADENCE Virtuoso, Spectre, Multisim, Pspice
- Excel, MS Word, PowerPoint



SDM INSTITUTE OF TECHNOLOGY, UJIRE

Department of Electronics and Communication Engineering

EXPERIENCE

- HOD at Dept. of ECE, SDM Institute of Technology (Ujire) **Oct-2022 to Present**
- ASSOCIATE PROFESSOR at Dept. of ECE, SDM Institute of Technology (Ujire) **May-2024 to Present**
- ASSISTANT PROFESSOR **May-2012 to Apr 2024**
- LECTURER **July-2009 to Apr-2012**
- GRADUATE ENGINEER **Sep-2006 to Sep-2007**
- RESEARCH ASSOCIATE **Aug-2005 to Aug-2006**

EDUCATION

- PH.D. ON DESIGN AND ANALYSIS OF RECONFIGURABLE FRACTAL MICROSTRIP ANTENNA FOR MULTI-BAND WIRELESS APPLICATIONS at Visvesvaraya Technological University (VTU) **2023**
- M.E. IN ELECTRONICS at UVCE (Bengaluru) **2011**
- B.E. IN ELECTRONICS AND COMMUNICATION ENGINEERING at SJMIT (Chitradurga) **2005**

RESEARCH AND PUBLICATIONS

- Number of Quality Journal Published **7**
- Number of Conference Papers **2**
- Number of Patents Granted/Published **2**

WORKSHOPS/FDPs ATTENDED IN LAST 5 YEARS

- FDPs: **2**
- Workshops: **6**

SUBJECTS HANDLED

Computer Networks, Python Programming, C++, Verilog HDL, Analog Electronic Circuits, Network Analysis, Basic Electronics, Digital Switching Systems

MISCELLANEOUS

- Institute level Coordinator for examinations for a period of 4 years
- Invited speaker at various colleges
- Reviewer for reputed journals
- Awarded grant money for KSCST student projects
- Student projects selected for Anveshana and numerous VTU competitions
- Institute level AICTE activity coordinator